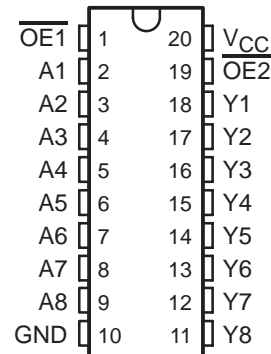


SN74ABT541B-Q1 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 150 V Using Machine Model (C = 200 pF, R = 0)
- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})

PW PACKAGE
(TOP VIEW)



description

The SN74ABT541B octal buffer and line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tape and reel	SN74ABT541BIPWRQ1	AB541IQ1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



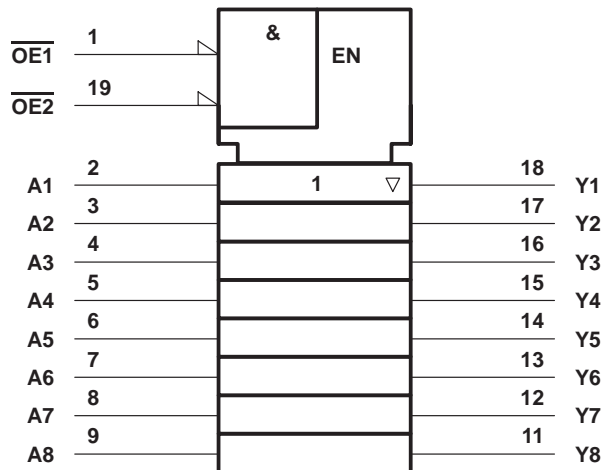
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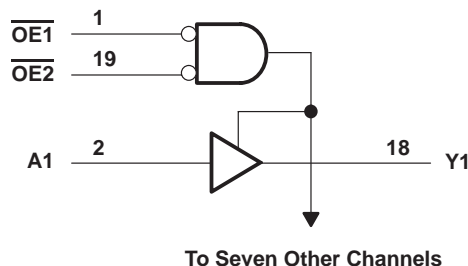
SN74ABT541B-Q1 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2)	128°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			MIN	MAX	UNIT
		MIN	TYP†	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2	-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5	V	
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		
	V _{CC} = 4.5 V, I _{OH} = -32 mA	2			2		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 64 mA			0.55	0.55	V	
V _{hys}			100			mV	
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1	±1	μA	
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50	±50	μA	
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50	±50	μA	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10	10	μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-10	-10	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100	±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V			50	50	μA	
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-140	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			5	250	250	μA
				22	30	30	mA
				1	250	250	μA
ΔI _{CC} §	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5	1.5	1.5	mA
				50	50	50	μA
				1.5	1.5	1.5	mA
C _i	V _I = 2.5 V or 0.5 V			3		pF	
C _o	V _O = 2.5 V or 0.5 V			6		pF	

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	Y	1	2	3.2	1	3.6	ns
t _{PHL}			1	2.6	3.5	1	3.9	
t _{PZH}	\overline{OE}	Y	2	3.5	4.5	2	4	ns
t _{PZL}			1.9	4	5.1	1.9	5.9	
t _{PHZ}	\overline{OE}	Y	2.2	4.4	5.4	2.2	5.8	ns
t _{PLZ}			1.5	3	4	1.5	4.4	
t _{sk(o)} ¶					0.5	0.5	ns	

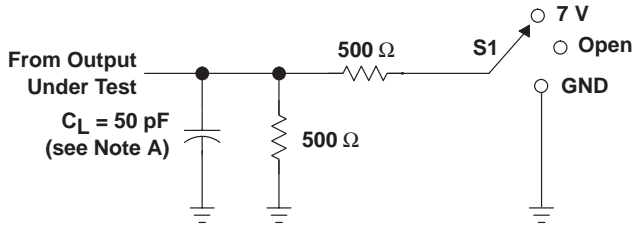
¶ Skew between any two outputs of the same package switching in the same direction



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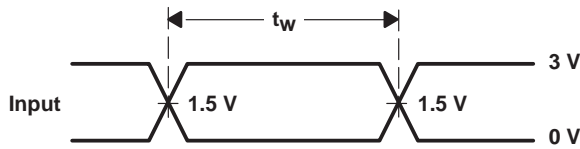
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PARAMETER MEASUREMENT INFORMATION

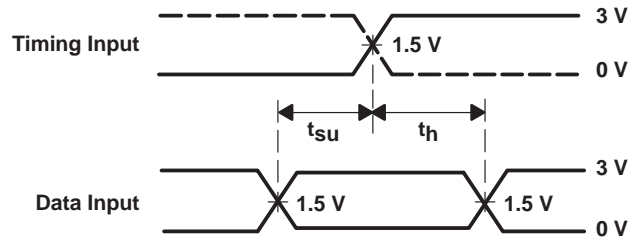


LOAD CIRCUIT

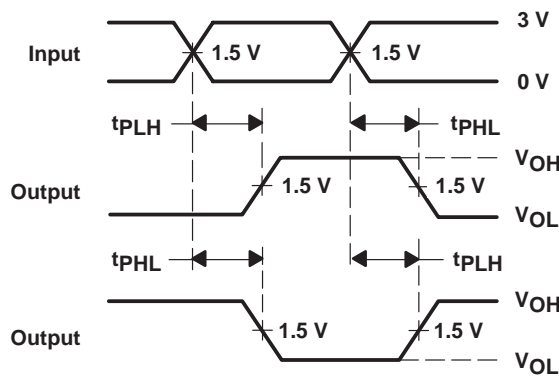
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



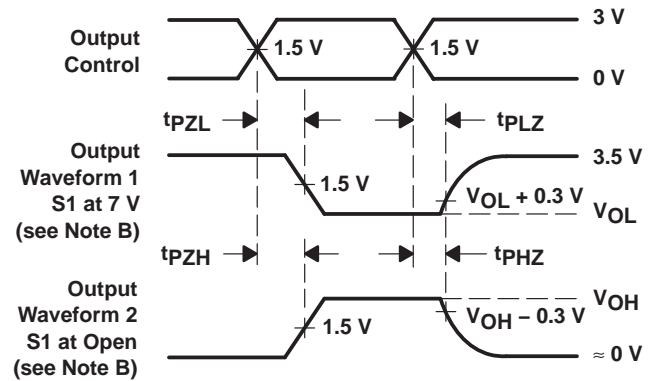
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ABT541BIPWRQ1	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74ABT541B](#)
- Enhanced Product: [SN74ABT541B-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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